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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WILSON, YOLANDA L	
ART UNIT	PAPER NUMBER
2184	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/724,839	SCHUBERT ET AL.	
	Examiner	Art Unit	
	Yolanda Wilson	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-13 and 15-26* is/are rejected.

7)☒ Claim(s) *6,14,27 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2356710* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 6,14,27,28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3,5,7,10-13,15-22,24,25 rejected under 35 U.S.C. 102(b) as being anticipated by Dervisoglu. As appears in claim 1, Dervisoglu discloses a trigger processing unit for monitoring trigger events and issuing a trigger action based on one or more of the monitored trigger events in section 4.1.1 on page 6, "Logic analyzer Trigger circuit (LAT):..." Dervisoglu discloses at least one probe circuit coupled between the integrated circuit hardware product and said trigger processing unit in section 4.1.1 on page 6, "Logic Analyzer Probes (LAP)..." Dervisoglu discloses a configuration register that stores configuration information for use in configuring said trigger processing unit or said at least one probe circuit in section 4.1.1 on page 7, "Said multiplexing circuits use dedicated flip-flops to control their operations so that scan operations are used to configure (i.e. program) the LAPs as desired." Dervisoglu discloses a communication controller operatively connected to said configuration

register to provide external access to said configuration register by the debugger system in section 4.1.1 on page 8, "The Logic Analyzer Interface circuit may rely on existing capability to execute serial scan operations in order to configure the LAP and LAT circuits as well as to empty the contents of the LAM after data has been captured in it."

4. As per claims 2,12, Dervisoglu discloses at least one probe circuit coupled to a region of the electronic circuit design within the integrated circuit hardware product to yield one or more signals for sampling or patching in section 4.1.1 on page 6, "Each LAP can be designed so that data is captured into a flip-flop that operates under the (fastest) on-chip system clock."

5. As per claim 3, Dervisoglu discloses a status register that stores status information pertaining to the electronic circuit design within the integrated circuit hardware product in section 4.1.1 on page 8, "In one mode of operation the LAM [Logic Analyzer Memory] can function as a circular buffer such that data is captured continuously until the trigger condition has been met and a pre-defined number of cycles have elapsed." Dervisoglu discloses said communication controller is operatively connected to said status register to provide external access to said status register by the debugger system in section 4.1.1 on page 8, "The Logic Analyzer Interface circuit may rely on existing capability to execute serial scan operations in order to configure the LAP and LAT circuits as well as to empty the contents of the LAM after data has been captured in it."

6. As per claim 5, Dervisoglu discloses said at least one probe circuit includes a plurality of probe circuits in section 4.1.1 on page 6, "Several LAPs could be selectively combined together to form a LAP channel."

7. As per claim 7, Dervisoglu discloses said electronic monitoring circuit further being automatically coupled to the electronic circuit design within the integrated circuit hardware product on page 10, Figure 9.

8. As per claims 10,17,24, Dervisoglu discloses the monitored trigger event include current trigger events and previous trigger events in section 4.1.1 on page 6, "Logic analyzer Trigger circuit (LAT)..."

9. As per claim 11, Dervisoglu discloses a trigger processing unit for monitoring trigger events and issuing a trigger action based on one or more of the monitored trigger events in section 4.1.1 on page 6, "Logic analyzer Trigger circuit (LAT):..." Dervisoglu discloses at least one probe circuit coupled between the integrated circuit hardware product and said trigger processing unit in section 4.1.1 on page 6, "Logic Analyzer Probes (LAP)..." Dervisoglu discloses a status register that stores status information pertaining to the electronic circuit design within the integrated circuit hardware product in section 4.1.1 on page 8, "In one mode of operation the LAM [Logic Analyzer Memory] can function as a circular buffer such that data is captured continuously until the trigger condition has been met and a pre-defined number of cycles have elapsed." Dervisoglu discloses said communication controller is operatively connected to said status register to provide external access to said status register by the debugger system in section 4.1.1 on page 8, "The Logic Analyzer Interface circuit may rely on existing capability to

execute serial scan operations in order to configure the LAP and LAT circuits as well as to empty the contents of the LAM after data has been captured in it."

10. As per claim 18, Dervisoglu discloses a trigger processing means for monitoring trigger events and issuing a trigger action based on one or more of the monitored trigger events in section 4.1.1 on page 6, "Logic analyzer Trigger circuit (LAT):..." Dervisoglu discloses at least one probe circuit means for monitoring at least one signal of the electronic circuit design within the integrated circuit hardware product in section 4.1.1 on page 6, "Logic Analyzer Probes (LAP)..." Dervisoglu discloses said communication means for providing external access to said electronic monitoring circuit by the debugger system in section 4.1.1 on page 8, "The Logic Analyzer Interface circuit may rely on existing capability to execute serial scan operations in order to configure the LAP and LAT circuits as well as to empty the contents of the LAM after data has been captured in it."

11. As per claim 19, Dervisoglu discloses configuration means for storing configuration information for use in configuring said trigger processing means or said at least one probe means in section 4.1.1 on page 7, "Said multiplexing circuits use dedicated flip-flops to control their operations so that scan operations are used to configure (i.e. program) the LAPs as desired."

12. As per claim 20, Dervisoglu discloses a communication means provides external access to said configuration means in section 4.1.1 on page 8, "The Logic Analyzer Interface circuit may rely on existing capability to execute serial scan operations in order

to configure the LAP and LAT circuits as well as to empty the contents of the LAM after data has been captured in it."

13. As per claim 21, Dervisoglu discloses a status register means for storing status information pertaining to the electronic circuit design within the integrated circuit hardware product in section 4.1.1 on page 8, "In one mode of operation the LAM [Logic Analyzer Memory] can function as a circular buffer such that data is captured continuously until the trigger condition has been met and a pre-defined number of cycles have elapsed."

14. As per claim 22, Dervisoglu discloses said communication means provides external access to said status register means in section 4.1.1 on page 8, "The Logic Analyzer Interface circuit may rely on existing capability to execute serial scan operations in order to configure the LAP and LAT circuits as well as to empty the contents of the LAM after data has been captured in it."

15. As per claim 25, Dervisoglu discloses circuitry that implements functionality of said integrated circuit product and customized instrument circuitry that enables internal signals produced by said circuitry to be examined and/or modified in section 4.1.1 on page 6, "One of the most effective features that can be included in an SoC for use in design verification is to integrate some of the functionality of a Logic Analyzer directly on the IC itself...Logic Analyzer Probes..."

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 4,13,23,26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dervisoglu in view of Whetsel (USPN 6378093B1). As appears in claims 4,13,23, Dervisoglu fails to explicitly state an analog-to-digital converter coupled between said at least one probe circuit and the electronic circuit design within the integrated circuit hardware product to provide analog-to-digital conversion.

Whetsel discloses in column 29, lines 55-59, "...an integrated circuit 2350 includes an analog to digital converter (ADC) 2352 connected, in test mode, to a scan collector circuit 2354 at its digital output and to an integrated circuit pad or core terminal 2356 at its analog input."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have an analog-to-digital converter coupled between said at least one probe circuit and the electronic circuit design. A person of ordinary skill in the art would have been motivated to have an analog-to-digital converter coupled between said at least one probe circuit and the electronic circuit design because an analog-to-digital converter is useful in converting signals from analog to digital whenever a circuit has analog signals and digital signals that need to be converted for processing.

18. As per claim 26, Dervisoglu fails to explicitly state circuitry includes analog and digital portions and said customized instrumentation circuitry enables internal signals produced in either the analog or digital portions of said circuitry to be monitored or patched.

Whetsel discloses in column 29, line 67 – column 30, lines 1-3 "this test is programmed to repeat the steps of inputting analog input to the ADC, converting the analog input into a digital output, and outputting the digital output to a test for inspection."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have circuitry includes analog and digital portions and said customized instrumentation circuitry enables internal signals produced in either the analog or digital portions of said circuitry to be monitored or patched. A person of ordinary skill in the art would have been motivated to have circuitry includes analog and digital portions and said customized instrumentation circuitry enables internal signals produced in either the analog or digital portions of said circuitry to be monitored or patched because circuits can have analog and digital signals and those signals need to be monitored for any errors or faults.

19. Claims 8,9,15,16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dervisoglu in view of Kawamura et al. (USPN US005801956A). As appears in claims 8,15, Dervisoglu fails to explicitly said electronic monitoring circuit is derived from a HDL description of the electronic circuit design.

Kawamura et al. discloses in column 1, lines 26-28, "HDL enables the direct description of detailed timing information and logic synthesis and operation verification can be conducted easily."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have an electronic monitoring circuit being derived from a HDL description of the electronic circuit design. A person of ordinary skill in the art would have been motivated to have an electronic monitoring circuit being derived from a HDL description of the electronic circuit design because HDL is a well known language that is used in the designing of integrated circuits. Kawamura et al. discloses in column 1, lines 20-24, "Since it is necessary in such integrated circuits to design a logic circuit with gates numbering more than five hundred thousand, the current mainstream practice is to perform design by using the HDL."

20. As appears in claims 9,16, Dervisoglu fails to explicitly state said electronic monitoring circuit is automatically created by an instrumentor.

Kawamura discloses in column 2, lines 48-59, "once the specifications of a logic circuit (LSI) are determined (S101), the HDL description is prepared according to the specifications (S102), and functional verification is performed (S103)... If the hardware is determined to be difficult to implement, the process returns to the step for preparing the HDL descriptions (S 102), while when high feasibility is involved, its logic synthesis is performed, and the process enters the LSI prototyping stage (S105)."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have an electronic monitoring circuit is automatically

created by an instrumentor. A person of ordinary skill in the art would have been motivated to have an electronic monitoring circuit is automatically created by an instrumentor because an instrumentor is used to in the creation and verification of a hardware circuit by way of using HDL description for a circuit design.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda Wilson whose telephone number is (703) 305-3298. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

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